REMARKS

Applicants respectfully request favorable reconsideration of this application as amended.

The title of the invention has been amended, as required, to be more clearly indicative of the claimed invention.

Without acceding to the rejection under 35 U.S.C. § 102(b), each of the independent claims under consideration has been amended to clarify the invention intended to be claimed. Claim 1, for example, has been amended to clarify that the recited potential pairs are used by the first and second logic gates in an active operation mode. Thus, as amended, Claim 1 recites a semiconductor integrated circuit comprising a first logic gate using, as an operation power source in an active operation mode, a first pair of potentials having a relatively small potential difference; and a second logic gate using, as an operation power source in the active operation mode, a second pair of potentials having a relatively large potential difference, wherein substrate potentials of MIS transistors are commonly used by the first and second logic gates.

Regarding Horiguchi et al., note that in the cited arrangement of Fig. 37, the switches Ss and Sc are closed

in the active operation mode so that the circuits L41 and L43 utilize the same potential difference (Vcc-Vss) as an operation power source, the additional potentials via resistors Rc and Rs being utilized only in the standby (low power consumption) mode.

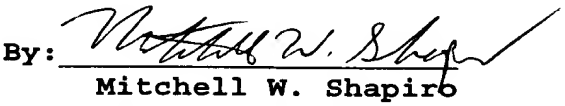
Accordingly, Applicants respectfully submit that the claims distinguish patentably from Horiguchi et al. and that the rejection under §102(b) should therefore be withdrawn.

The Examiner's indication of allowable subject matter in Claims 13, 15, 17 and 19 is noted with appreciated. These claims have been retained in dependent form in view of the allowability of their respective base claims as discussed above.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this

paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

By: 
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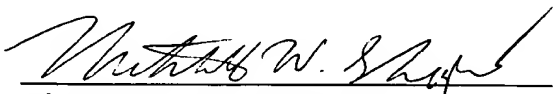
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Marked-up copy of the Amended Claims (09/855,660):

1. (Amended) A semiconductor integrated circuit comprising:

a first logic gate using, as an operation power source in an active operation mode, a first pair of potentials having a relatively small potential difference; and

a second logic gate using, as an operation power source in said active operation mode, a second pair of potentials having a relatively large potential difference,

wherein substrate potentials of MIS transistors are commonly used by said first and second logic gates.

6. (Amended) A semiconductor integrated circuit comprising:

a first logic gate using, as an operation power source in an active operation mode, a first pair of potentials having a relatively small potential difference; and

a second logic gate using, as an operation power source in said active operation mode, a second pair of potentials having a relatively large potential difference,

wherein [ach of] said first and second logic gates [has an] have MIS transistors, and a well r gion [of the]

in which an MIS transistor [in which] of said first logic gate is formed and a well region [of the] in which an MIS transistor [in which] of said second logic gate is formed are made common [every] for each conduction type.

7. (Amended) A semiconductor integrated circuit comprising:

a first logic gate using, as an operation power source in an active operation mode, a first pair of potentials having a relatively small potential difference; and

a second logic gate using, as an operation power source in said active operation mode, a second pair of potentials having a relatively large potential difference,

wherein [each of] said first and second logic gates [has an] have MIS transistors, and a well region [of the] in which an MIS transistor [in which] of said first logic gate is formed and a well region [of the] in which an MIS transistor [in which] of said second logic gate is formed are electrically [made conductive every] connected for each conduction type.

12. (Amended) A semiconductor integrated circuit comprising:

a first logic gate using, as an operation power source in an active operation mode, a first pair of a high potential and a low potential; and

a second logic gate using, as an operation power source in said active operation mode, a second pair of a high potential and a low potential having a potential difference larger than that of said first potential pair,

wherein a substrate potential of an MIS transistor in said first logic gate and that of an MIS transistor in said second logic gate are common to each other, and

at least said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by said substrate potential.

16. (Amended) A semiconductor integrated circuit comprising:

a first logic gate connected to a first pair of a high potential line and a low potential line in an active operation mode; and

a second logic gate connected to a second pair of a high potential line and a low potential line in said active operation mode, said second lin pair having a potential difference larger than that of said first potential line

pair,

wherein a substrate potential line is commonly used for supplying a substrate potential to an MIS transistor of said first logic gate and for supplying a substrate potential to an MIS transistor of said second logic gate, and

at least said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by said substrate potential.

20. (Amended) A semiconductor integrated circuit having a circuit region in which a number of logic gates each having an MIS transistor are arranged on a semiconductor substrate,

wherein said circuit region has a well region <u>including portions</u> shared by a substrate potential [every] <u>for each</u> conduction type of [an] MIS transistor,

a first logic gate using, as an operation power source <u>in an active operation mode</u>, a first pair of potentials having a relatively small potential difference and a second logic gate using, as an operation power source <u>in said active operation mode</u>, a second pair of potentials having a relatively large potential difference ar formed in said

well region,

in said well region, a p-type well [region] portion in which an n-channel type MIS transistor is formed and an n-type well [region] portion in which a p-channel type MIS transistor is formed are adjacent to each other, and

metal lines for supplying said first pair of potentials, said second pair of potentials, and [a] substrate potentials are arranged on said well region.

37. (Amended) A design data recording medium on which design data for [designing] forming an integrated circuit [to be formed] on a semiconductor chip [by using a computer] is recorded so as to be [read] readable by [said] a computer, the design data comprising:

first mask pattern data for determining a figure pattern for forming a first logic gate to which an operation power source is supplied, in an active operation mode, from a first pair of potential lines having a relatively small potential difference and a substrate potential is supplied from a substrate potential line on said semiconductor chip; and

second mask pattern data for determining a figure pattern for forming [on said semiconductor chip] a second

logic gate to which an operation power source is supplied, in said active operation mode, from a second pair of potential lines having a relatively large potential difference and a substrate potential is supplied from a substrate potential line.

38. (Amended) A design data recording medium on which design data for designing an integrated circuit to be formed on a semiconductor chip is recorded so as to be [read] readable by [said] a computer, the design data [comprises] comprising:

first function description data for determining a function of a first logic gate to which an operation power source is supplied, in an active operation mode, from a first pair of potential lines having a relatively small potential difference and a substrate potential is supplied from a substrate potential line; and

second function description data for determining a function of a second logic gate to which an operation power source is supplied, in said active operation mode, from a second pair of potential lines having a relatively large potential difference and a substrate potential is supplied

from a substrate potential line connected to said substrate potential line.